Roll No.

ANNA UNIVERSITY (UNIVERSITY DEPARTMENTS)

B.E / B. Tech (Full Time) END SEMESTER EXAMINATIONS – NOV/DEC 2024

ELECTRICAL & ELECTRONICS ENGG

EE 8304 Linear Integrated Circuits (Regulation 2012)

Time: 3 Hours | Answer ALL Questions | Max. Marks 100

PART- A (10 x 2 = 20 Marks)

Q.No	Questions	Marks
1.	How is SiO_2 layer useful during IC fabrication?	2
2.	What are the advantages of ICs over discrete components' based circuits?.	2
3.	What is 'V to I converter'? Give an application for the same.	2
4.	Sketch the circuit diagram of an OPAMP based integrator? Also show that its output voltage is proportional to the integration of input voltage.	2
5.	Define the input offset current of an OPAMP? What is the technique followed to reduce the error due to this, especially in a high gain inverting amplifier?	2
6.	How does the current mirror circuit help improve the CMRR of an OPAMP?	2
7.	Draw the circuit diagram of a positive clipper circuit. You may assume either positive or negative V_{ref}.	2
8.	Draw the circuit diagram of a 2-bit flash-type ADC. How many comparators would be required in a 6-bit flash type ADC?	2
9.	What are the characteristics expected from an ideal OPAMP ?	2
10.	Define the capture range of a PLL? How is it different from its lock-in range?	2

PART- B (5 x 16 = 80 Marks)

(Q. No 11 is Compulsory)

Q.No	Questions	Marks
11.	i) Draw the circuit diagram of the following circuits based on OPAMP: inverting amplifier, non-inverting amplifier and differential amplifier. Also, discuss the voltage-shunt feedback concept or voltage-series feedback concept, using one of these circuits as example? ii) Explain why 'masking and etching' are repeatedly carried out during the IC fabrication process? Illustrate with an example circuit. (8 + 8)	16
12.	a) i) Draw the internal block diagram of the 555 timer IC and briefly discuss its internal features. ii) Design a 555 timer based astable multi-vibrator for a frequency of 500 Hz. The duty-ratio required is 0.7. (8 + 8)	16
	OR	
	b) Design a 2nd order Low pass Filter with cut-off frequency of 600 Hz. Derive an expression for the cut-off frequency of this OPAMP based circuit. Compare the Butterworth filter characteristics with other types.	16
13.	a) Along with the circuit diagram and derivation of relevant expressions, discuss the operation of anyone oscillator circuit that can be used to generate a sine wave of 400 Hz frequency	16
	OR	

	b) i) Along with the internal block diagram, discuss the operation of the voltage controlled oscillator IC 566. Also derive an expression for its output frequency. How is this VCO useful in a PLL circuit?	16
	ii) What is an 'analog multiplier" circuit? How is it useful in implementing a Phase Locked Loop circuit? (8 + 8)	
14	a) I) Discuss the operation of a dual slope type ADC? How is it advantageous when compared to other types of ADCs?	16
	ii) What is a 'sample and hold' circuit? How is it different from a peak detector circuit? (12 + 4)	
	OR	
	b) i)What is an R-2R ladder type DAC ? Considering such a DAC with 3 –bit capacity, show that output analog voltage is proportional to the input bit pattern by considering the input bit patterns 011_2 and 110_2.	16
	ii) What is an 'instrumentation amplifier'? (12 + 4)	
15.	a) Along with block diagram, principle of operation and applica ion examples, discuss in detail ANYTWO of the following topics: i) Voltage regulator IC 7805. ii) Power amplifier LM 380. iii) Function generator IC.	16
	OR	
	b) How does an OPAMP based tri-angular waveform generator circuit operate? Design a tri-angular waveform generator circuit for a frequency of 600 Hz; after deriving the required expressions. Assume the peak voltage required to be 60% of the supply voltage. What modification would you carry out in the above circuit to change the waveform as shown in the figure below? (Note that the positive and negative slopes of the tri-angular waveform are now different.)	16

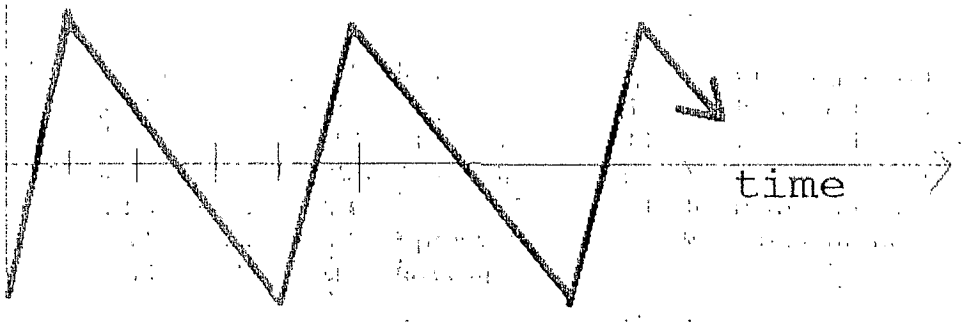

Figure for Q 15 B.